SEVENTH FRAMEWORK
PROGRAMME

ICT Project no. 258547

ATEMOX

Advanced Technology Modeling
for Extra-Functionality Devices

Final Publishable Summary

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Executive summary

Previous European projects with major contributions by the current partners helped to bring process simulation to a state which allows in industrial environments a sufficiently accurate simulation of doping profiles in advanced CMOS technologies. Important electrical characteristics of core CMOS devices can be predicted from scratch or with a minimum calibration effort.

However, concepts towards low-power electronics, smart power applications, CMOS image sensors, and CMOS derivatives providing extra functionalities were not sufficiently supported by TCAD. This concerns especially the prediction of leakage currents in such or parasitic devices caused by electrically active defects that remain after processing, and alternative doping techniques like plasma immersion ion implantation, low-temperature implantation, diversified cocktail implants and laser annealing which are considered for low-leakage ultra-shallow junctions. The lack of suitable models that can be used in the early stages of industrial R&D inhibited the necessary cost reduction in the development of devices for which Europe is still at the forefront. ATEMOX now developed many of the missing models and implemented and included them into the Sentaurus TCAD platform of Synopsys so that they are of immediate value to the European semiconductor industry. The integrated models were finally evaluated by STMicroelectronics with respect to industrial needs.

To reach the ambitious goals, a consortium of European companies active in complementary fields of competence (STMicroelectronics: device manufacturing, Synopsys: TCAD software, Exico, IBS: equipment production, Probion, Semilab: characterization) and leading European research institutes (CNRS-LAAS/CEMES, CNR-IMM, ETH-Zurich, Fraunhofer-IISB, Univ. Newcastle) has been formed to expertly cover all fields from experiment via characterization and modelling to simulation as well as to ensure full coverage of the value chain.

As a primary output of ATEMOX, a variety of models implemented and integrated in the Sentaurus TCAD platform have been released already during the period of the project from July 2010 to November 2013 or will be released shortly. The results obtained were disseminated via six poster presentations and 24 oral presentations of which four were invited. In addition, the work resulted in 24 articles in peer-reviewed journals and conference proceedings.

Project context and objectives

The main intention of ATEMOX is to extend the capabilities of technology-computer aided design (TCAD) to the prediction of leakage currents and to the alternative doping processes considered for a reduction of leakage currents. To understand what has led us to the idea, it is necessary to describe the status and main opportunities from the point of view of the European nanoelectronics industry, the state of TCAD in industrial environments, and its potential role in strengthening the competitiveness of Europe’s nanoelectronics industry. This is briefly done in the following.

Due to the increased costs especially of research and development (R&D), the next generations of basic nanoelectronics technologies will be developed within a few major global R&D alliances. The real strength of the European nanoelectronics industry lies in its high product mix and shifted from the “More Moore” domain towards applications like low-power electronics, smart power applications, mixed-mode, RF and analogue IC applications, CMOS image sensors, and other CMOS derivatives providing extra functionality to the basic nanoelectronics technology. Going from core CMOS technology to CMOS derivatives implies a change of paradigm in R&D. While core CMOS technology aims at improved performance, particularly switching speed, it is mandatory for CMOS derivatives to find a trade-off between the traditional view of device ‘performance’ (switching speed, ...) and objectives like leakage current, standby power consumption, and dark currents. In fact, for CMOS image devices, the dark current is as important a feature as the restitution of the signal under illumination and for mobile communication, power consumption is even more an argument than traditional ‘performance’. For all these applications, because of the rapidly changing requirements of customers, time-to-market is a decisive advantage that European nanoelectronics industry needs to maintain especially versus competitors in Asia.

Previous European projects under coordination and with major contributions by the current partners helped to bring process simulation to a state which allows in industrial environments a sufficiently accurate simulation of doping profiles in advanced CMOS technologies. Important electrical characteristics of core CMOS devices can now be predicted from scratch or with a minimum calibration effort. This enables a significant reduction of development costs and time. For the main-stream technologies, according to the 2011 Update of the International Technology Roadmap for Semiconductors (ITRS), TCAD may reduce development costs and time by roughly one third, with a tendency to rise. The prediction of leakage currents is significantly less matured because of the extreme challenges associated with. Simulations of off-state currents at ST with the state-of-the-art Sentaurus TCAD platform failed to predict the basic trends even for the core CMOS technologies from 65 nm down to 32 nm available. This made TCAD virtually useless for the design of applications where a trade-off between performance and leakage has to be found. A further challenge was that alternative doping techniques like plasma immersion ion implantation, low-temperature implantation, diversified cocktail implants, and laser annealing considered particularly for CMOS derivatives were significantly less understood than the processes used for core CMOS technologies. When not optimized, these processes may lead to the formation of electrically active defects with deep levels in the band gap that aggravate leakage currents. In consequence, the lack of suitable models that can be used in the early stages of industrial R&D inhibits the reduction of development time by the use of TCAD and, consequently, the necessary cost reduction in the development of devices for which Europe is still at the forefront.

Formulation, implementation, and integration of predictive models for leakage currents in CMOS derivatives and for the respective technologies were the main challenges of this project. They were also the basis of the detailed scientific objectives of the ATEMOX project. The project objectives resulted from a critical assessment of TCAD requirements for CMOS derivatives by ST. These requirements were discussed with the research institutes and Synopsys with respect to their possible achievement and the establishment and implementation of the respective physical models into industrially used TCAD software. Additional industrial partners, all SMEs with a clear record of innovation, were invited to join the project on the basis of their complementary expertise and usually their world-wide leadership. Using synergies between the partners, in most cases already successfully exploited in previous RTD projects, our team was able to master these extreme challenges associated with the three project objectives formulated:

Objective 1 (scientific): Investigation of the formation of electrically active defects responsible for leakage currents and the respective alternative doping techniques

Objective 2 (strategic): Implementation and integration of the models developed into commercial releases of the Sentaurus TCAD platform of Synopsys

Objective 3 (technological): Demonstration that the models developed, implemented and integrated into the Sentaurus TCAD platform are able to predict threshold voltages, short-channel effects and leakage currents in CMOS derivatives based on the 32 nm technology developed in the CATRENE project UTTERMOST.

Main S&T Results

The examples given in the following should be seen as a glimpse on the achievements of the project.

Diffusion during low temperature anneals

Fabrication processes for CMOS derivatives include low temperature process steps for gate stack and spacer formation, such as deposition of amorphous silicon, polysilicon, oxide, or nitride layers. These processes have thermal budgets ranging from 500°C to 800°C with duration from 1 sec to 200 minutes. For such thermal budgets, in inert atmosphere only little if any dopant diffusion can be observed. However, the same thermal treatments when associated with deposition, oxidation or nitridation may lead to active dopant redistribution. Up to now there had been no systematic evaluation of the validity of the diffusion and clustering models in TCAD simulations for low temperature annealing in different ambients.

In ATEMOX, silicon samples with δ-layers were fabricated. They were then subjected to annealings at 750 and 800 °C. These temperatures are so low compared to traditional silicon processes that very long annealing times had to be used, as long as 2.5 days at 750 °C. These profiles were then analyzed by SIMS.

In order to model the diffusion of the δ-layers, the models already implemented in Sentaurus Process were used. However, the most advanced model, named ChargedReact, had to be used. A new calibration was proposed for the low temperatures. An example of the calibration is presented in Figure 1 for boron and in Figure 2 for phosphorus.

With these calibrated parameters, it is now possible to simulate diffusion of boron and phosphorus at lower temperatures. This enables the simulation of the fabrication process of CMOS derivatives.

Outdiffusion in spacer materials

A crucial region in any MOS-like device is the lightly-doped drain (LDD), which controls many of the targeted electrical characteristics. Dopants may segregate or diffuse out of the silicon into the spacer or stress memory techniques (SMT) materials located above it. The control of the active profiles in term of steepness, resistivity and short-channel effects is highly dependent of the evolution of doping profiles in the channel, LDD and oxide/nitride stacks.

Figure 3 shows that the doping profile in this region is strongly dependent on the type and conditions of the deposition of the spacer material. Up to now, it was not possible to simulate these phenomena correctly.

In ATEMOX, experiments were carried to understand dose loss and segregation of dopants from the silicon into the overlying layers during all following thermal processes. The interactions of dopants and their co-diffusion under various types of deposition were studied.

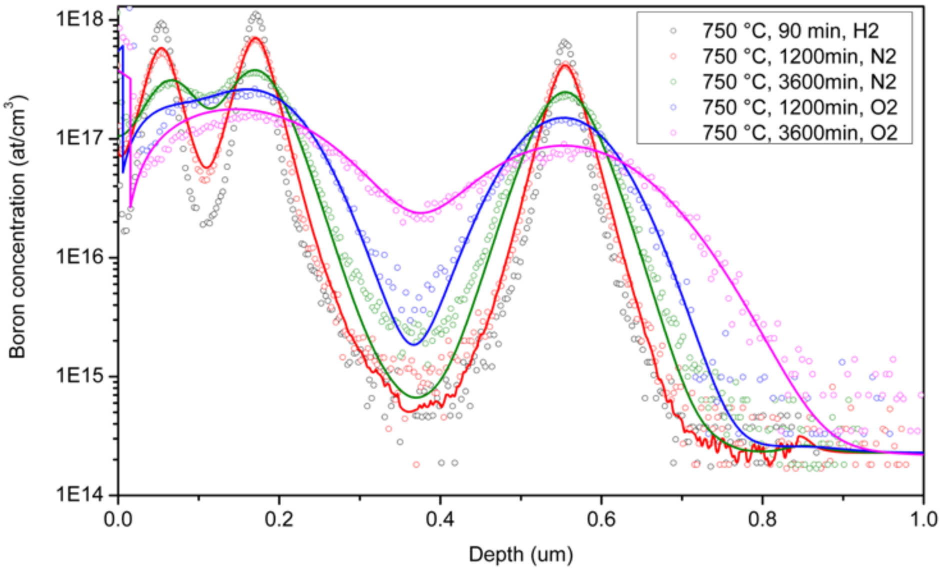

Figure 1: Results for the modelling of the broadening of boron δ-layers with an initial peak concentration of 2·10^{18} cm^{-2} during annealing at 750 °C in N_2 and O_2 atmospheres.

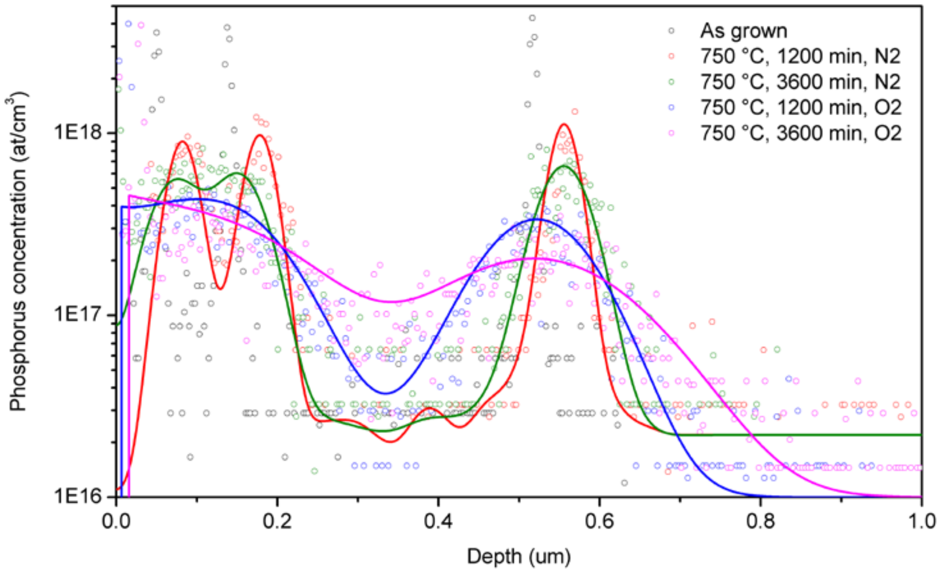

Figure 2: Results for the modelling of the broadening of phosphorus δ-layers with an initial peak concentration of 2·10^{18} cm^{-2} during annealing at 750 °C in N_2 and O_2 atmospheres.

With the help of these experiments, the interaction between doping atoms, oxygen atoms and hydrogen related species were modeled. This model was calibrated and implemented in Sentaurus Process. Figure 4 shows the good agreement between experiments and simulations that can be achieved with this model.

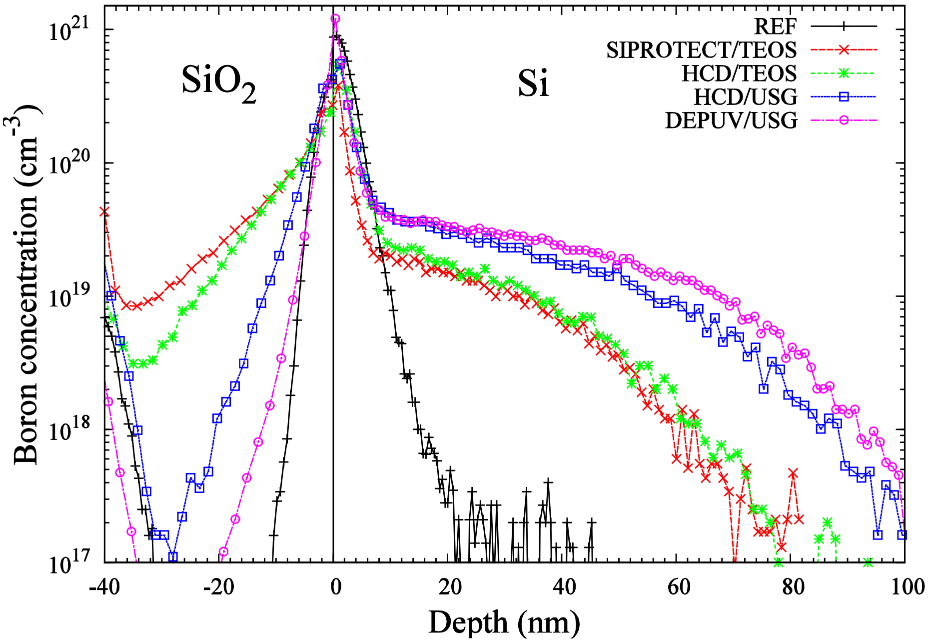

Figure 3: Boron SIMS results for different nitride/oxide spacer stack combinations annealed at 1000 °C 2 min, in addition to REF HCD/TEOS reference sample before annealing.

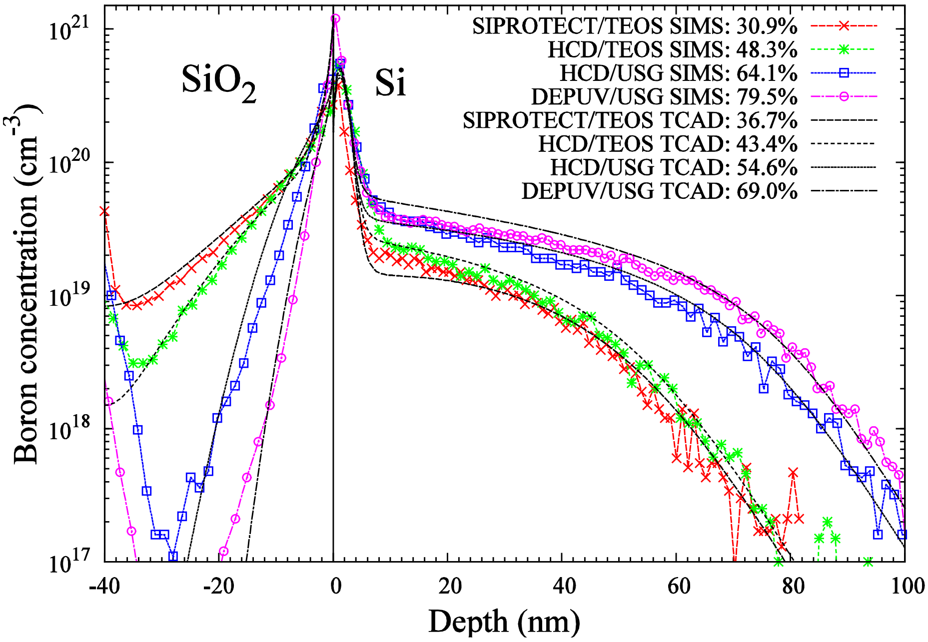

Figure 4: Boron SIMS profiles versus TCAD results for different nitride/oxide spacer stack combinations using. Final percentages of the boron dose loss in silicon are also given in the legend.

Dopant diffusion in high-k/metal gate stacks

High-k dielectrics and metal gates have been investigated for many years, but most of these investigations have focused on immediate technological questions (fabrication, characterization) or on explaining the aspects of the physical phenomena observed (e.g. by ab-initio simulations).

In ATEMOX, the influence of high-k dielectrics on silicon was first studied. Electrical characterization of the gate capacitances were first performed after various treatments of high-k gate stacks. The outcome was that the doping variation at the gate stack/silicon interface was in a 10% range while taking into consideration the lowest and the highest thermal budgets. As a consequence, the thermal budget had only little effect on the diffusion and segregation from the high-k/Metal gate stack to silicon. On the contrary, the thermal budget had a noticeable influence on lanthanum and aluminum diffusion in the gate stack. These effects were then further studied.

A first Lanthanum diffusion model was proposed. The results were published by Essa et al.[1] and are shown in Figure 5.

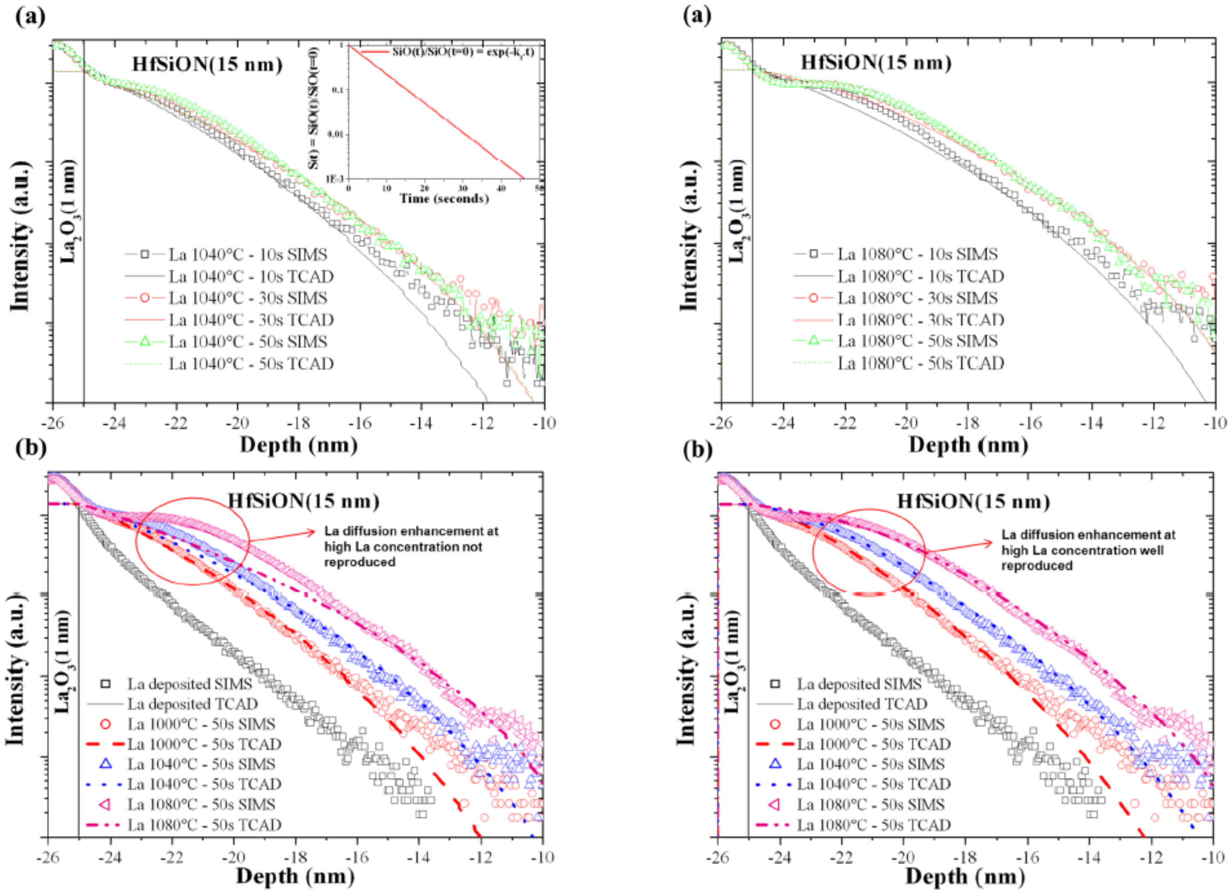

Figure 5: La SIMS versus TCAD profiles for various anneal conditions, from [Essa2013], fig. 5 and 6.

A good agreement can already be seen for most profiles. This first model is a very important milestone for the availability of models for high-k dielectrics in Sentaurus Process.

The correlation between the La diffusion and the voltage shift observed in nMOS devices was investigated, too. The results were published by Hackenberg et al.[2] Figure 6 shows an example of these results.

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[1] Z. Essa et al.: Evaluation and modeling of lanthanum diffusion in TiN/La2O3/HfSiON/SiO2/Si high-k stacks, Appl. Phys. Lett 101, 182901 (2012)

[2] M. Hackenberg et al., “Influence of La on the electrical properties of HfSiON: From diffusion to Vth shifts”, Microelectronic Engineering 109 (2013) 200–203

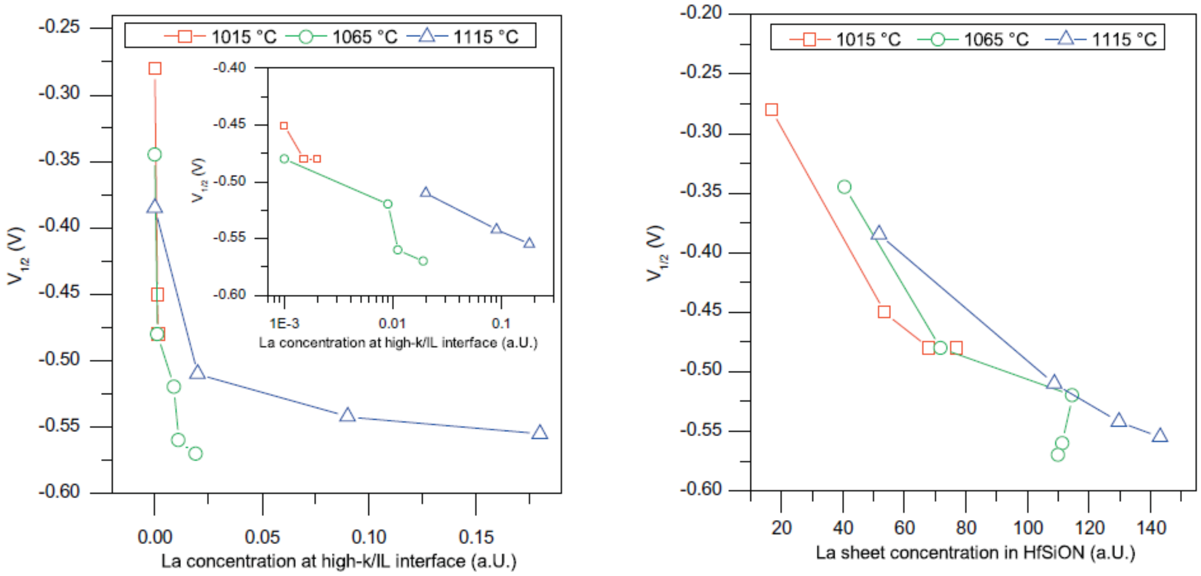

Figure 6: Nonlinear correlation of the La concentration at the interface HfSiON/SiO2 to VT (left) and approximately linear correlation of the La sheet concentration in the HfSiON to the shift in VT (right). Each point corresponds to a different annealing time (from Hackenberg2013])

Several explanations were proposed for the observed behavior. Like for La diffusion, this result is an important milestone for the implementation of models for high-k in Sentaurus Process.

Models for Plasma Immersion Ion Implantation

Thanks to the collaborative work achieved in ATEMOX project, two 1D/2D models to simulate BF3 plasma doping has been developed[34]. These two models based Monte-Carlo approach have been used and excellent agreement with as-implanted doping profiles observed by SIMS is achieved as depicted Figure 7.

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[3] A. Burenkov, A. Hahn, Y. Spiegel, H. Etienne, and F. Torregrosa: Simulation of BF3 Plasma Immersion Ion Implantation into Silicon, IIT 2012

4 Z. Essa, F. Cristiano, Y. Spiegel, P. Boulenc, M. Quillec, N. Taleb, A. Burenkov, M. Hackenberg, E. Bedel-Pereira, V. Mortet, and C. Tavernier: BF3 PIII modelling: implantation, amorphisation and diffusion, IIT 2012

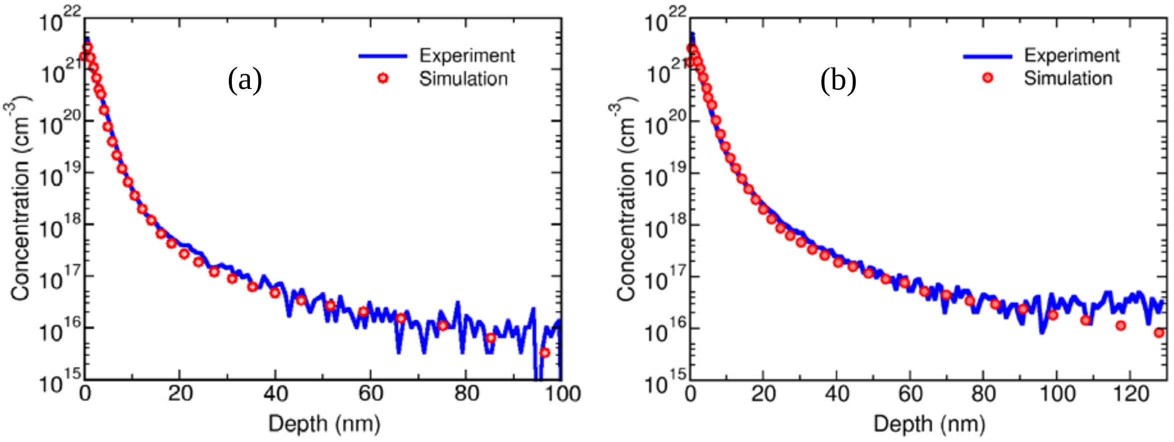

Figure 7: As-implanted Boron profiles in BF_3 implanted silicon samples: Comparison of the Monte-Carlo based simulation with improved model vs SIMS for 1 keV (a) and 2 keV (b) plasma extraction voltages

Models describing defect and dopant behaviour during annealing of plasma-implanted samples have been implemented in Synopsys Sentaurus TCAD software and excellent results are obtained, see Figure 13 further down. These models well account for dopant deactivation leading to god agreement with Hall measurements as illustrated in Figure 8[5].

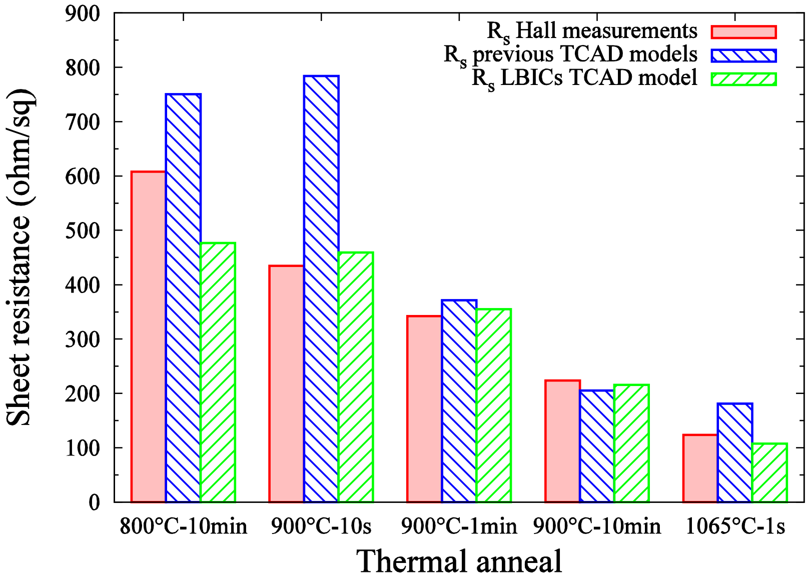

Figure 8: P+/N BF_3 PIII junctions' sheet resistance extracted from Hall effect measurements for the different thermal anneals. Comparison with adv-calibration featuring LBICs model or not.

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[5] F. Cristiano, Z. Essa, Y. Qiu, Y. Spiegel, F. Torregrosa, J. Duchaine, P. Boulenc, C. Tavernier, O. Cojocaru, D. Blavette, D. Mangelinck, P. F. Fazzini, M. Quillec, M. Bazizi, M. Hackenberg, S. Boninelli: Implantation-induced structural defects in highly activated USJs: Boron precipitation and trapping in pre-amorphised silicon, IWJT 2012

An 1D/2D/3D analytical model has been developed [6]and several applications of these simulations on 3D structures as trench doping have been performed (see Figure 9).

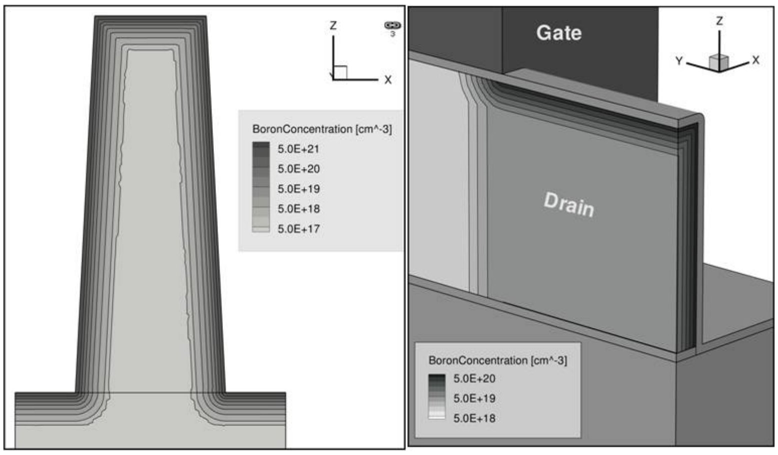

Figure 9: Right: BF_3 implanted boron distribution in a trench-like structured silicon sample (trench depth is 180 nm) simulated using analytical model for a dose of $1{\cdot}10^{15}$ cm^{-2} and an extraction voltage of 1 keV. Left:Analytically simulated boron distribution after a BF_3 plasma immersion ion implantation into a 25 nm FinFET device for a dose of $1{\cdot}10^{14}$ cm^{-2} and an extraction voltage of 1 keV

A second modelling approach has been conducted based on an extended Monte-Carlo model for PIII. Starting with the characterization of 3D structures, analysis to highlight the dopant presence were carried out using TEM/EFTEM/STEM methods in order to investigate the doping conformity in trench type structures. The developed numerical model includes all relevant phenomena causing the evolution of plasma exposed substrates and the implanted Boron profile resulting from BF2 PIII implantation is shown in Figure 10.

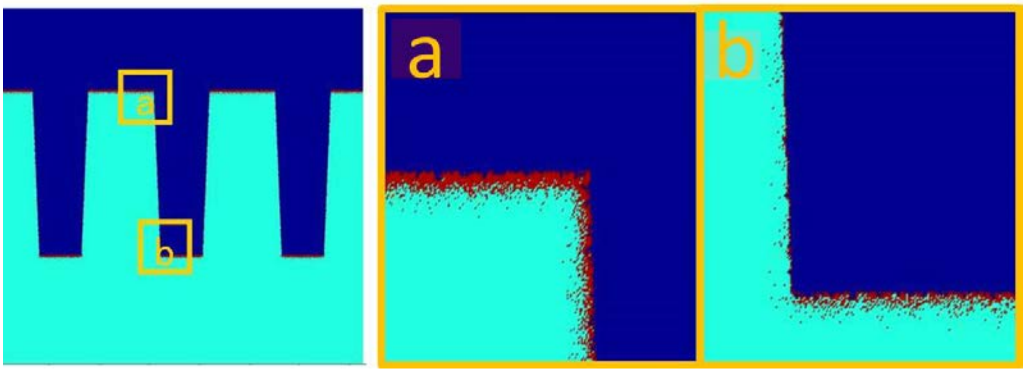

Figure 10: Left, considered trench structure; Right, zoom view of the simulation with ion angular distribution assumed equal to the neutral one.

“Large BICS” in highly B-doped implanted by PIII

In the frame of ATEMOX, one of the major findings was the observation of large unconventional (001) oriented defects which were suspected to be B-rich interstitial clusters (BICs). It

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[6] . Burenkov, A. Hahn, Y. Spiegel, H. Etienne, and F. Torregrosa: Simulation of BF_3 Plasma Immersion Ion Implantation into Silicon

has been first evidenced by HRTEM, as shown in Figure 11; in highly Boron doped samples resulting from high dose BF3 plasma immersion ion implantation which the Boron concentration at the amorphous/crystalline silicon interface is above the solubility limit.

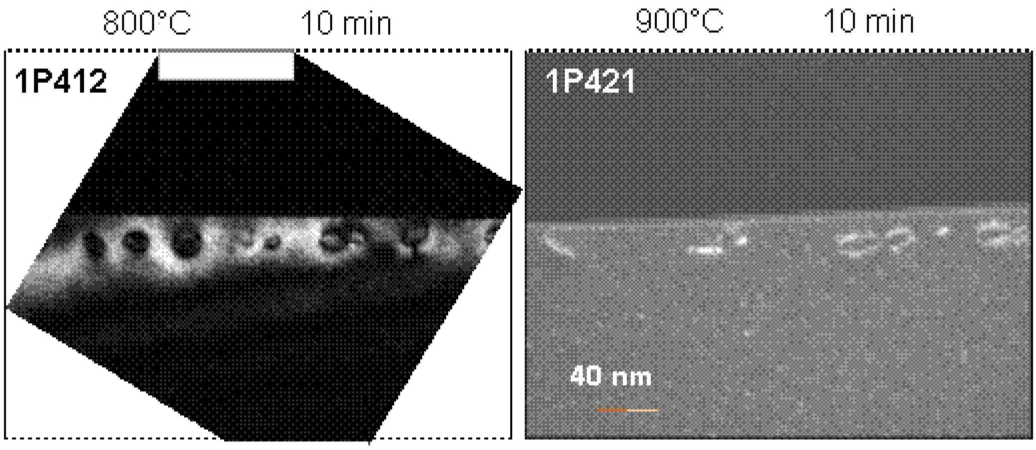

Figure 11: Cross-sectional TEM images of BF_3 10kV 5E14 at/cm² implanted samples

Large boron interstitial clusters continuum modeling

Continuum modelling of LBICs containing hundreds to thousands of boron and silicon interstitial atoms cannot be held by simulating all LBICs sizes, and a more CPU time efficient method has to be developed for TCAD requirements. Thus, a moments approach already used for classical {311} and (111) dislocation loops interstitial EOR defects developed by Synopsys[7] was used. In Figure 12, we show an atomistic view diagram explaining the LBICs model where the three moments[8]

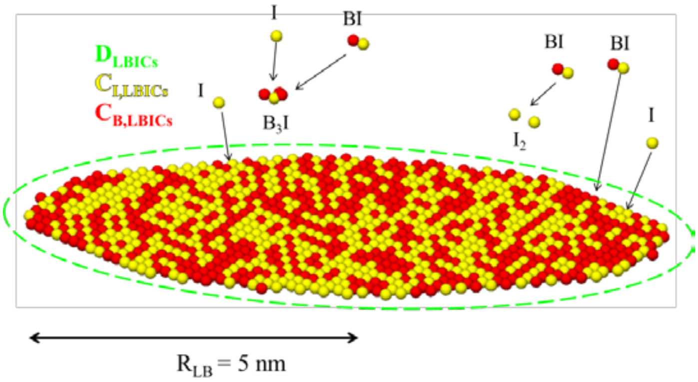

Figure 12: Atomistic view diagram representing the formation of a (001) dislocation loop: the LBIC is formed following the reaction of free I with a small BIC B_3I and free I and BI with a small interstitial cluster I_2. The three moments of the model are the LBICs density (dashed circle), number of boron atoms and number of silicon interstitial atoms. LBICs can also grow in size R_{LB} following the capture of I and BI.

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[7] N. Zographos, C. Zechner and I. Avci, Mat. Res. Soc. Symp. Proc. 994, 297 (2007).

[8] Z. Essa, F. Cristiano, O. Cojocaru-Mirédin, D. Mangelinck, D. Blavette, S. Duguay, N. Zographos, P. Boulenc and C. Tavernier: Continuum modelling of large boron-interstitial-clusters in silicon

Using the LBICs model, annealed samples (800°C, 900°C, 1065°C) were simulated and TCAD results are given in Figure 13. Thanks to the addition of the LBICs model to the ones of AdvancedCalibration featuring 311 and Dislocation loops formation, a much better agreement is found between SIMS and TCAD boron diffused profiles mainly for high thermal budgets, including boron peak behind the A/C interface and its slow dissolution when increasing the thermal budget[9].

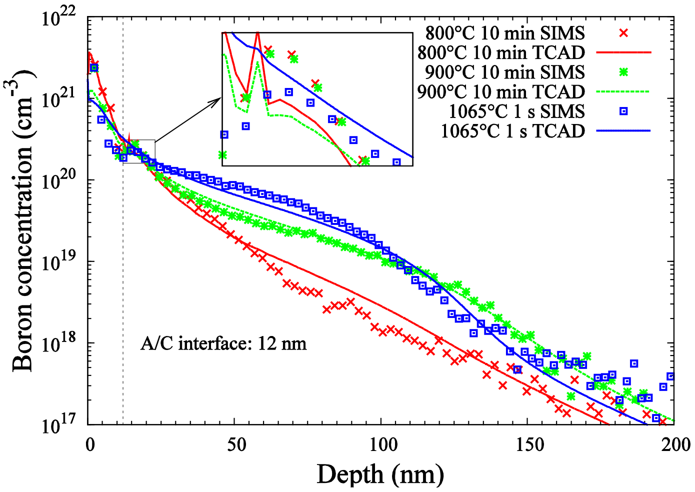

Figure 13: Boron SIMS versus TCAD profiles using the LBICs model following a BF_3 plasma implant at 10 kV 5.10^{15} cm^{-2} annealed at 800°C 10min, 900°C 10min and 1065°C 1s.

Excimer Laser modeling

One of the objectives of ATEMOX project was to investigate and model the excimer laser anneal (MLA) technique in order to enable further TCAD based optimization of such tool process condition. A large database of experimental data has been constituted including SIMS, sheet resistance and Hall measurements and complementary Electrochemical Capacitance-Voltage Profiling (ECVP) measurements, Model-Based Infrared (MBIR) metrology, Current-Voltage measurements with Elastic Material probe (FastGate® FCV) and Mercury probe (Hg MCV) and TEM pictures to characterize the doping profiles, amorphization depth, EOR defect location and type. Based on the knowledge acquired, physical models have been developed featuring:

Continuous models for thermal and phase evolution as well as dopant diffusion under Laser annealing were developed and calibrated: a first model based on enthalpy[10] and adsorption and second model based on phase field and two-state diffusion[11]. The results of the calibrated models, reported in Figure 14 for the 2.6 J/cm² case, are in excellent agreement with the experimental results.

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[9] Z. Essa, F. Cristiano, Y. Spiegel, Y. Qiu, P. Boulenc, M. Quillec, N. Taleb, N. Zographos, E. Bedel-Pereira, V. Mortet, A. Burenkov, M. Hackenberg, F. Torregrosa, and C. Tavernier, “Large boron-interstitial clusters modelling in BF_3 plasma implanted silicon”, to be published in Physica Status Solidi (2013).

[10] M. Hackenberg, P. Pichler, K. Huet, R. Negru, J. Venturini, G. Fisicaro, and A. La Magna: Modeling boron profiles after pulsed excimer laser annealing, IIT 2012

[11] G. Fisicaro, K. Huet, R. Negru, J. Venturini, M. Hackenberg, P. Pichler, and A. La Magna: Dynamics of dopant redistribution in molten silicon caused by laser irradiation, IIT 2012

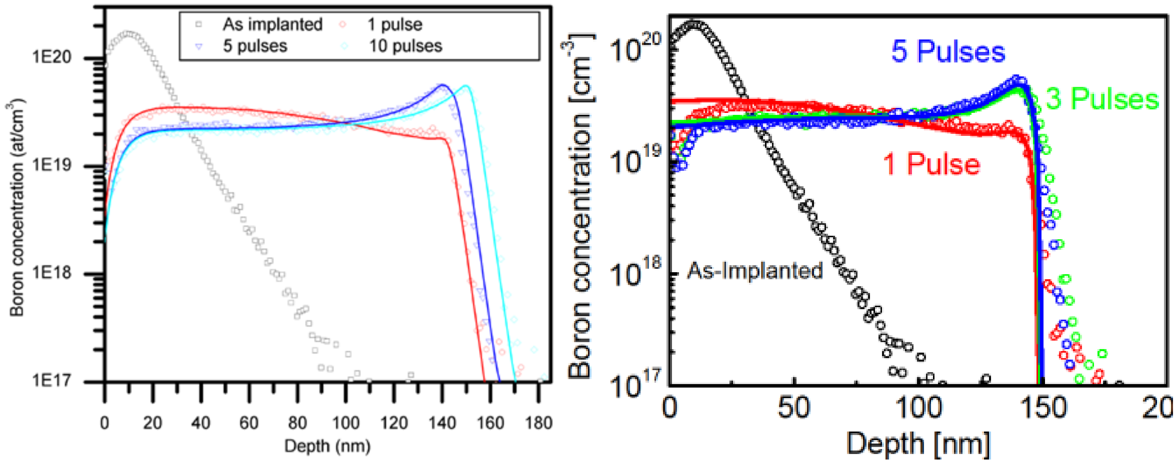

Figure 14: Comparison of the measured (symbols) and simulated (lines) profiles after 1, 5, and 10 pulses of 2.6 J/cm2. Left: Adsorption approach from Fraunhofer, right: 2-state diffusion approach by CNR-IMM.

A coupled Phase-Field/Kinetic Monte Carlo (PF-KMC) approach has been developed at CNR-IMM to investigate the correlation between dopant activation and defect's evolution in boron implanted silicon under excimer laser irradiation. Results reported in Figure 15 are in fair agreement with the experimental measurements.

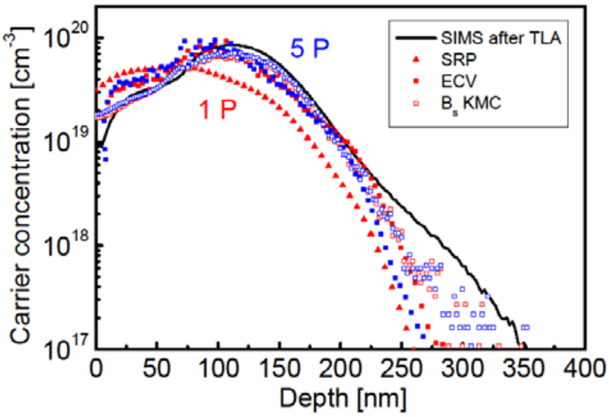

Figure 15: Experimental results from SRP (filled triangles) and ECV (filled squares) measurements for 2.3 J/cm2 laser fluence for single (red data) and multi-pulse (blue) processes. Simulated substitutional boron atoms (red empty square). SIMS profiles as implanted (dark line) and after LTA (red dashed).

“Large BICS” in highly B-doped Si annealed by Excimer Laser

The investigation of Excimer Laser performed in the frame of ATEMOX has demonstrated that, as expected, high dopant activation and excellent crystal quality was achieved in the molten layers. Moreover, a dopant pile-up near the maximum melt depth was observed in the partial melt cases. Intensive HRTEM analysis, illustrated by the results shown in Figure 16 and Figure 17, evidenced the presence of “Large BICS” in case of melted sampled annealed with energy density of 2.6J/cm2 and partially melted samples annealed with 1.5 J/cm2 ED.

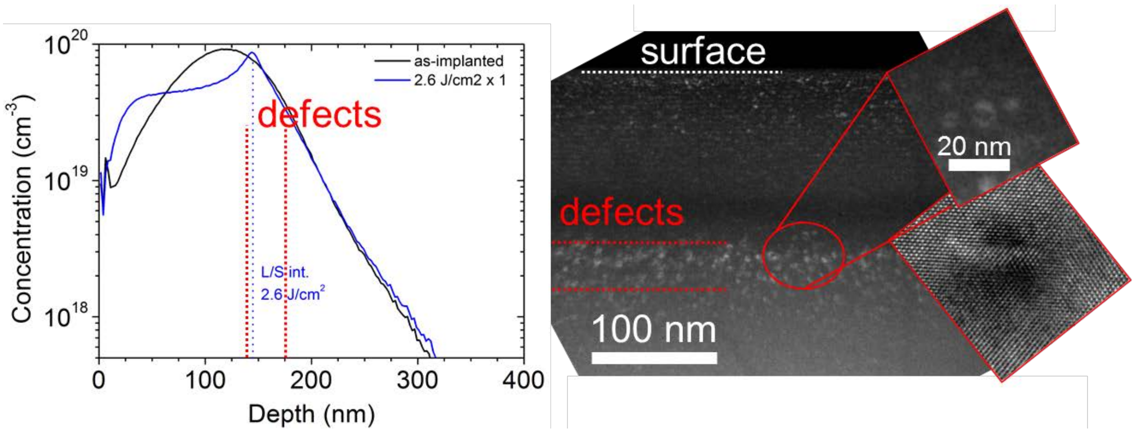

Figure 16:.SIMS Boron profile (left) and cross section Weak Beam TEM images (right) from the sample laser annealed with 2.6 J/cm2 (1 shot).

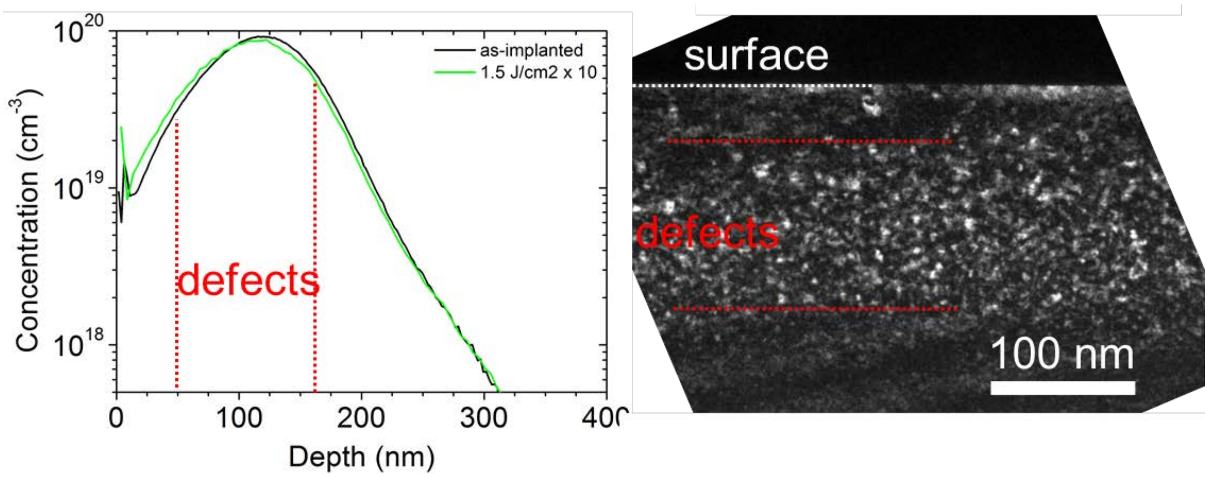

Figure 17: SIMS Boron profile (left) and cross section Weak Beam TEM images (right) from the sample laser annealed with 1.5 J/cm2 (10 shots, non-melt).

Despite the evidence of “Large BICS” on partially molten samples, Fast-Gate and Mercury EM-Probe I-V measurements didn’t evidence impact on leakage currents.

Moreover, those “Large BICs” like loops have been observed in dedicated LTA silicon implanted samples. Therefore, the observed loops are not large BICs but would rather be large Si interstitial clusters potentially decorated by Boron atoms (in the B implanted cases).

Junctions leakage

Leakage current is among the crucial properties of today’s MOS devices. Every intention to decrease leakage currents in any structure requires a deep understanding of the underlying physics by which the various leakage mechanisms are governed and which processing steps lead to the occurrence of these mechanisms. In particular, most of the junction fabrication methods investigated within ATEMOX result in the formation of extended defects that are expected to have a major impact on the junction leakage currents. Our work therefore focused on the systematic study of the electrical characterisation of the process-induced defects and of the related junction properties. On the basis of the acquired knowledge from experiments, existing TCAD models were improved and new models were developed for the most relevant junction leakage mechanisms.

The investigation of the electrical properties of the fabricated junctions was based on the realisation of dedicated diode test structures allowing both reliable leakage current I-V measurements as well as the physical characterisation of the extended defects by Deep Level Transient Spectroscopy (DLTS).

Defect characterization

Experiments were first focused on small interstitial clusters (ICs) and {311} rod-like defects, typically formed during low thermal budget anneals (up to ~750°C). They were subsequently extended to larger dislocation loops (DLs) formed during annealing with higher thermal budgets. In all cases, the electrical impact of ion implantation defects was investigated both in n-type and p-type substrates, in order to provide a complete picture of all the deep levels introduced in the bandgap and hence support the development of leakage current physical models.

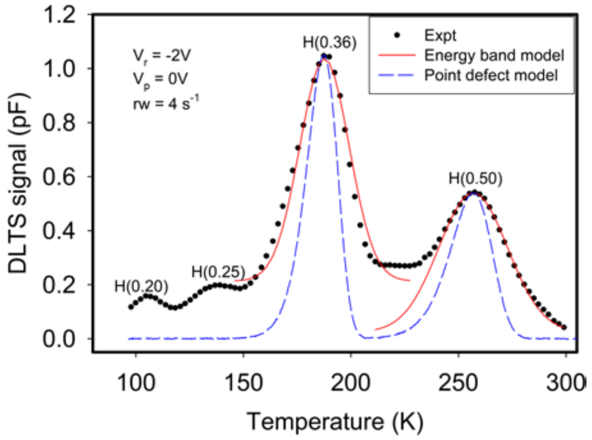

Figure 18: DLTS spectra of hole traps in the sample implanted with 1 x 10^{12} Si cm-2 and annealed at 500 °C for 1 h, (i) experimental data (solid circles), and after simulation with (ii) pointdefect model (dashed line) and (iii) defect band model (solid line).

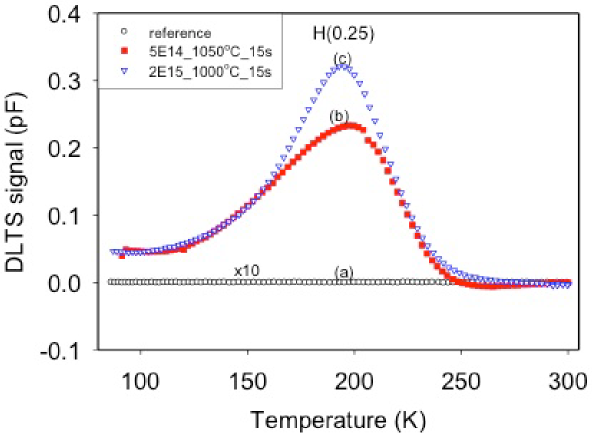

Figure 19: DLTS spectra of Ge implanted p-type samples. Implantation of Ge is implemented at different fluences of 5E14 cm^{-2} (red symbols) and 2E15 cm^{-2} (blue symbols). Black symbols represent the reference sample.

Our investigations allowed us to conclude that, in the upper part of the Si bandgap, there is no peculiar deep level associated to either small ICs or larger {311}s. Instead, they both introduce a similar electron-trap deep level located at $E_c - 0.54$ eV [12,13]. In the lower part of the bandgap, hole-traps with energy levels at $E_v + 0.36$ eV and $E_v + 0.50$ eV (cf. Figure 18) were associated to small ICs[14], which are similar to those previously observed for {311} defects in p-type Silicon[15]. As for larger DLs, they have been found to introduce a main electron trap level $E_c - 0.35$ eV and the hole trap level $E_v + 0.25$ eV (cf. Figure 19).

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[12] C. Nyamhere et al. AIP Conf. Proc. 1496 (2012) 171

[13] C. Nyamhere et al. J. Appl. Phys., 113 (2013) 184508

[14] C. Nyamhere et al. Phys. Status Solidi C (2013), doi:10.1002/pssc.201300204

[15] S. Libertino *et al*. PRB 63 (2001) 195206

Based on the systematic comparison between DLTS data and defect simulations, we also evidenced that the concentration of defect-related DLTS centers is closely related to the concentration of interstitials on the periphery of the structural defects rather than to the number of Si interstitial atoms they contain. This is shown in Figure 20 for ICs/{311}s and in Figure 21 for DLs. This is a very important experimental result to support the commonly accepted assumption that the extended defects are electrically active at their periphery, and which has been used in the subsequent modelling work.

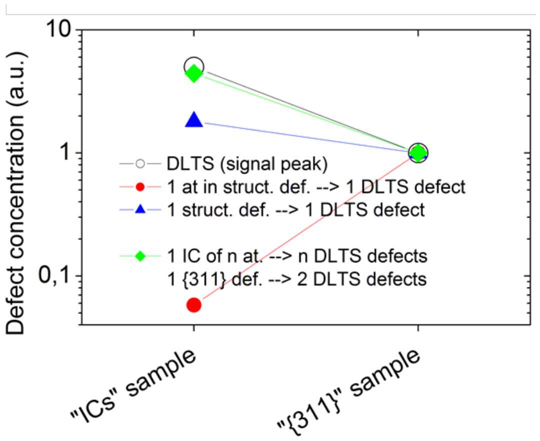

Figure 20: Defect concentrations obtained in the two investigated samples by DLTS measurements (black circles) or obtained by defect simulations according to different assumptions (filled coloured symbols, see text). The data are normalised with respect to the defect concentration in the {311} sample. cm^{-2} (ICs, triangles).

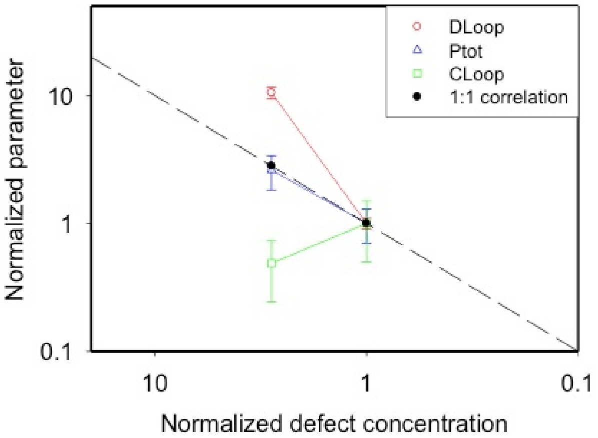

Figure 21: Normalised defect properties (Dtot, Ctot or Ptot) as a function of defect peak concentration extracted from DLTS for electron trap E(0.38) in samples implanted with 2 × 10^{15} Ge cm^{-2} annealed at 1000°C or 1100°C.

Leakage current measurements

While the DLTS measurements targeted the characterization of energy levels in the band gap, additional I(V)-measurements on these samples were conducted to find possible correlations between defect properties and leakage currents. Typical results are shown in Figure 22 and Figure 23. In the case of defects formed in n-type Silicon (Figure 22), the leakage current density (recorded at reverse bias of 0.5V) increases by 4 orders of magnitude (with respect to the non-implanted reference) when the sample is annealed at 1000^{o}C. After increasing the annealing temperature from 1000^{o}C to 1100^{o}C, there is an order of magnitude decrease in the leakage current, which is consistent with the corresponding decrease in dislocation loops density and/or the peripheral density of interstitials. Similarly, in the case of dislocation loops formed in p-type substrates (Figure 23), the leakage current increases in samples containing a higher density of dislocation loops (i.e. higher implant dose).

The main conclusions of these experiments can be summarised as follows:

- In the presence of implant-induced defects, the leakage current is strongly increased compared to reference non-implanted sample
- When the implant defects are located in the space charge region, the leakage current can be directly related to the electrical active defects in the band gap. In the case of interest of samples containing dislocation loops, the deepest levels E(0.38) and H(0.25), identified by DLTS, can therefore be directly related to the increase in leakage current.
- In the case when the defects are in the neutral region of the substrate they still contribute significantly to the leakage current, although the mechanism by which they contribute to leakage is unclear.

- In all cases, the defect-induced leakage current appears to be more closely related to the density of the existing structural defects (or to the density of the peripheral interstitials), rather than to the number of Si interstitial atoms they contain.

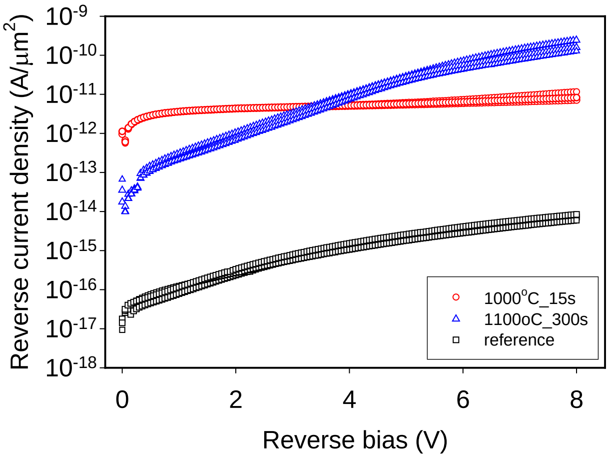

Figure 22: Reverse leakage current versus reverse bias in the n-type reference sample and pn-diode samples implanted with 2 x 10^{15} Ge cm^{-2} and annealed at 1000°C or 1100°C.

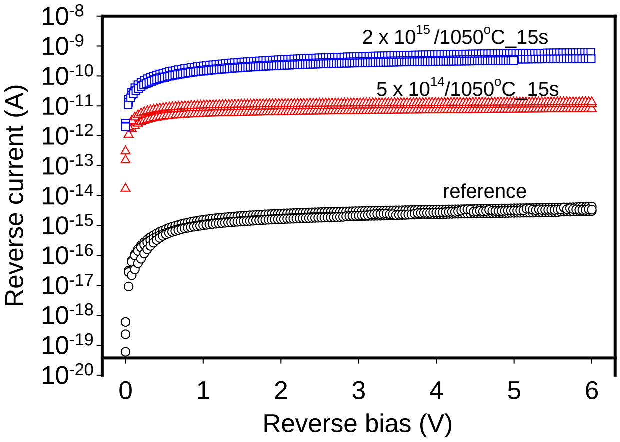

Figure 23: Leakage current measurements on p-type Schottky diodes with different implant doses and annealing at 1050°C.

Further measurements have been accomplished on industrial state-of-the-art samples. Conventional I(V)-measurements have been carried out by ST Crolles on structured samples. Destruction-free techniques as the Junction Photo Voltage (JPV) and Fast Gate Elastic Metal Probe technique have been used to obtain leakage characteristics of plain wafers.

Leakage modeling

To investigate deeper into the electrical nature of the extended defects, a DLTS simulation engine was developed and implemented at the ETH. This methodology combines the flexibility to test and apply new physical models for the interaction of the defect with the conduction and the valence band with the accuracy of the state-of-the-art industrial device simulator S-Device from Synopsys. The use of self-consistent electrostatics obtained from S-Device simulations for the DLTS simulations ensures realistic results.

Using the DLTS simulation methodology it was shown that the Coulomb repulsion is the most probable source for deviations from the characteristics of a point defect. Figure 24 shows the impact of varying Coulomb contributions on the DLTS signal. Furthermore, incorporating the Coulomb repulsion term into the capture and emission expressions of the defects reproduces the DLTS peak broadening observed in the experimental characterisations (see Figure 25).

Using the knowledge obtained about the electrical activity of the dislocation loop defects, device simulations have been conducted and the leakage currents found in the dedicated samples were reproduced after an adoption of the carrier capture cross sections to 10^{-14} cm^2. The field-dependence of the measurements, which is reproduced by the simulations with corrected defect profiles, shows the influence of the defect parameters as e.g. position and concentration.

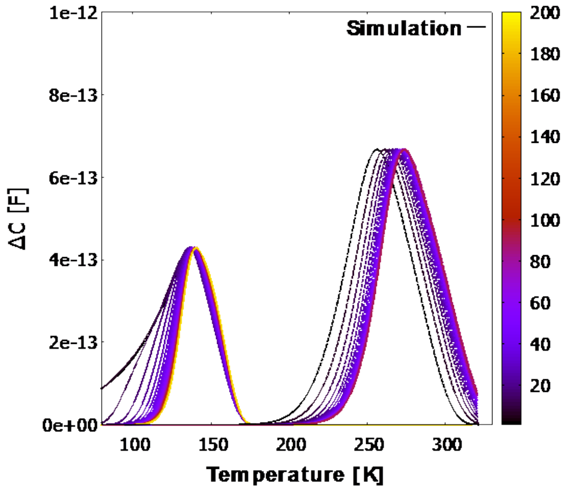

Figure 24: Simulation of the impact of a Coulomb repulsion on the DLTS signal of a {311} defect in dependence on the packing density of its periphery. A peak broadening and a shift of the peak to lower temperatures are observed with increasing Coulomb contributions.

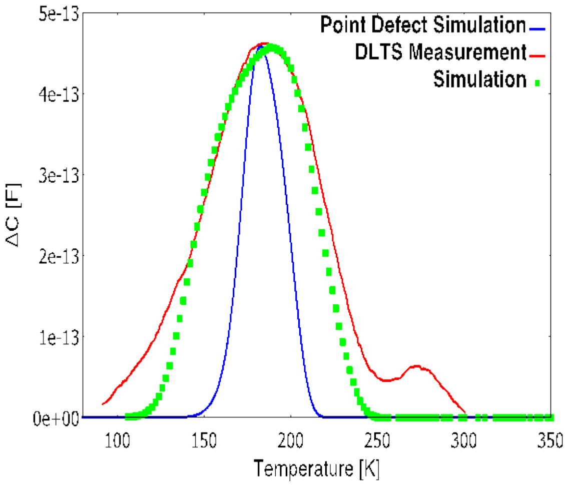

Figure 25: Comparison of a measured DLTS signal for Ge implanted DL samples with a point defect simulation and a DLTS simulation incorporating Coulomb repulsion. A single level is broadened by Coulomb contributions to the binding energy.

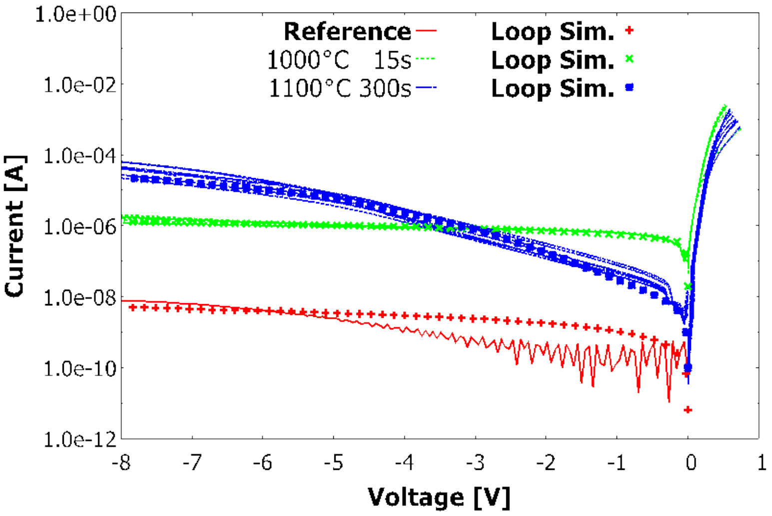

Figure 26 Leakage current simulations based on the defect distributions for dedicated P^+N junction samples. Defect parameters have to be scaled.

ATEMOX models included in Sentaurus Process

The process models developed within ATEMOX and the parameter calibration performed for ultra shallow junction design were evaluated by Synopsys for inclusion in the Sentaurus Process model library and in the “Advanced Calibration” set of recommended process models and parameters.

With the Synopsys TCAD Releases F-2011.09, G-2012.06, H-2013.03, and I-2013.12, a number of models and model calibrations developed within ATEMOX have been made available to users of Sentaurus Process world-wide and are described in the Sentaurus Process User Guide and the Advanced Calibration for Sentaurus Process User Guide.

These include:

- A model for melting laser annealing (MLA). The model has been implemented and tested in Sentaurus Process. An application note, *IGBT Characterization With Backside Melt Laser Annealing*, was created for TCAD Sentaurus as an example how to use the MLA model. The project demonstrates the simulation of MLA backside processing integrated in a 2D IGBT process simulation. The application note is public and available for download from Synopsys homepage via SolvNet®.
- A model for the diffusion and clustering of nitrogen. This calibration has been included as the new module "AdvancedNitrogenModel" to the AdvancedCalibration set of process models and parameters. The model can be used to investigate the impact of N co-doping in ultra shallow junction formation. A simulation result for implantation, clustering, diffusion and dose loss of N in absence of dopants is shown in Figure 27.

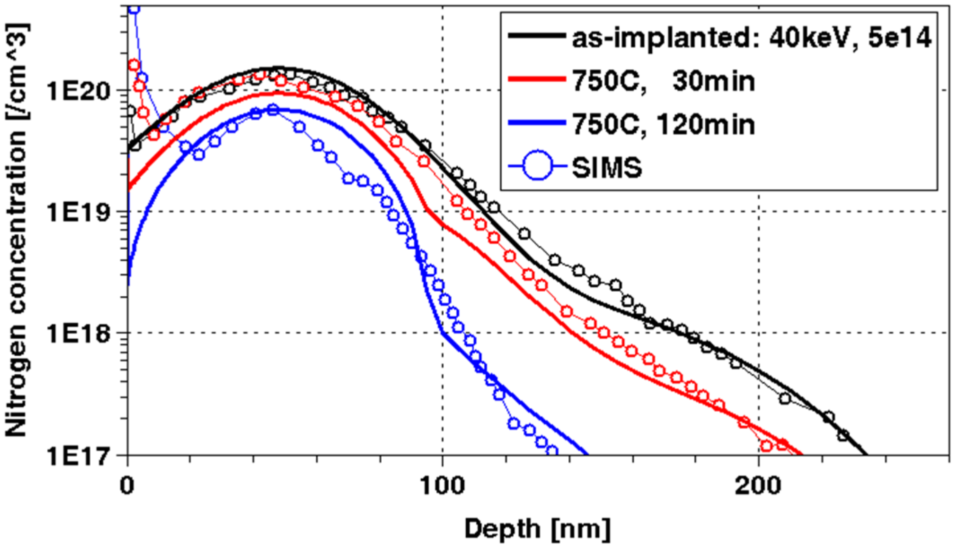

Figure 27: Nitrogen SIMS data (symbols) compared to process simulation results (lines) obtained with the nitrogen model developed and calibrated within the ATEMOX project. N was implanted at 40 keV with a dose of 5.0×10^{14} cm^{-2} and annealed at 750 °C for 30min or 120min. SIMS data are taken from Adam[16].

- A calibration for dopant redistribution during solid phase epitaxial regrowth (SPER) of silicon regions amorphized by ion implantation. This model allows the simulation of dopant diffusion in amorphous silicon (relevant for shallow B implants into preamorphized silicon) and the snow plow effect (some impurity species, such as indium are pushed towards the surface during SPER). The calibration of the SPER model has been integrated to the Advanced Calibration set of models and parameters as the optional module *AdvancedSPERModel*. An example for the snow plow effect of indium measured with SIMS and simulated with *AdvancedSPERModel* is shown in Figure 28.
- Improved formulas for the energy distribution and tilt angle distribution of plasma ions, which can be used in monte carlo simulation of plasma implantation steps.

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[16] L. S. Adam et al., *Diffusion of Implanted Nitrogen in Silicon at High Doses*, in MRS Symp. Proc., Si Front-End Processing–Physics and Technology of Dopant-Defect Interactions III, vol. 669, p. J3.10, January 2001.

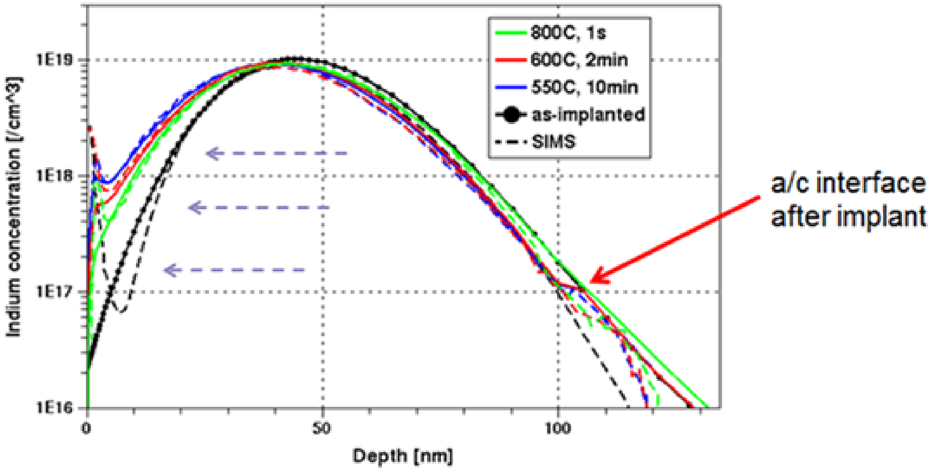

Figure 28: Indium profiles after implant into preamorphized silicon (black) and after solid phase epitaxial regrowth at different temperatures. SIMS data taken from Duffy et al.[17] (dashed lines) are compared to simulation results (lines) obtained with Sentaurus Process using *AdvancedSPERModel*. During SPER, indium is pushed towards the surface. The effect is strongest if SPER is performed at low temperature.

- Various improvements for the modelling of ultra shallow junction formations. For the following aspects of process modelling the Advanced Calibration set of models and parameters was improved based on the research conducted within the ATEMOX project, and leading to a significantly improved overall accuracy of Sentaurus Process:
  - Amorphization by ion implantation.
  - As-implanted boron profiles in silicon after low energy ion implantation.
  - Drift and diffusion of P and As in highly doped regions, for inert and oxidizing atmospheres.
  - Long-hop diffusion tail of phosphorus profiles annealed at low temperatures.

In addition, the impact of properly solving the Poisson equation in process simulation, not only inside silicon but also at MOS interfaces has been investigated and corresponding boundary conditions have become available in Sentaurus Process. The process modelling with quantum corrections for charge carrier density near material boundaries has also been investigated. In CMOS devices, a small but noticeable impact on simulated dopant distribution and device characteristics was demonstrated for both methods new in applied process simulation: Solving the Poisson equation in all materials, and applying quantum corrections to charge carrier density at MOS structures.[18]

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[17] R. Duffy et al., *Influence of preamorphization and recrystallization on indium doping profiles in silicon*, J. Vac. Tech. B 22, 3, 2004

[18] A. Tsibizov et al., “Influence of Poisson equation boundary conditions, and quantum corrections to carrier concentrations at material interfaces, in TCAD process simulation”, physica status solidi, accepted for publication.

Potential impact, main dissemination activities and exploitation of results

Potential impact

The project lead to a quantitative understanding and the establishment of quantitative models in a variety of aspects of process and device simulation that far exceed the state-of-the-art prior to ATEMOX.

In the area of process simulation, progress beyond state-of-the-art was achieved especially for critical processes and alternative doping processes considered for the fabrication of CMOS derivatives with well-controlled on-characteristics and leakage currents:

- Diffusion phenomena observed during processing at low temperatures, such as out-diffusion or in-diffusion of dopants at temperatures below 850 °C
- Dipole formation, interdiffusion, and dopant diffusion through high-k dielectrics
- Extended cocktail implants involving co-doping of arsenic and phosphorus and eventually carbon for n+ regions, activated by spike annealing and non-melt laser annealing
- Extended cocktail implants involving combinations of boron, fluorine, and carbon for p+ regions, activated by spike annealing and non-melt laser annealing
- Melting-laser processing
- Plasma immersion ion implantation
- Ion implantation at elevated and cryogenic temperatures

In contrast to previous work on doping processes for main-stream CMOS applications, progress was not only achieved for activation and diffusion, but also for the formation of electrically active defects with deep levels in the band gap.

In the area of device simulation, progress beyond the state-of-the-art was achieved for the modelling of leakage currents, in particular leakage currents caused by process-induced defects.

With the models developed for process and device simulation, European semiconductor industry will be able to save considerably development time and costs as for the core CMOS technologies by using TCAD early in the design of CMOS derivatives so that the respective electronic components and systems may be offered earlier and cheaper to the market. With the potential of TCAD to save about one third of the development time and costs also for CMOS derivatives as documented in the ITRS, the expected commercial potential of our proposal is substantial.

Main dissemination activities

Workshop at the E-MRS Spring Meeting

To facilitate the dissemination of ATEMOX results but also to get feedback on our work, a workshop on “Physics and technology of advanced extra functionality CMOS-based devices” has been organized at the Spring Meeting of the European Materials Research Society[19] from

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[19] http://www.emrs-strasbourg.com/index.php?option=com_content&task=view&Itemid=1583&id=592

May 27 to 30 in Strasbourg, France. The proceedings of the symposium were published as special issue (vol. 11, no. 1) of physica status solidi (c).

Public workshop for TCAD end-users:

A public workshop for TCAD end-users was organized by Synopsys and held on May 30th, 2013, at the E-MRS conference in Strasbourg, attended by 25-30 TCAD users. Various models developed during the ATEMOX project were presented and discussed with the audience. The slides presented at that workshop can be downloaded from the ATEMOX web page.[20]

Presentations at scientific conferences

16th International Conference on the Simulation of Semiconductor Processes and Devices, September 8-10, Osaka, Japan

- A. Burenkov, P. Pichler, J. Lorenz, Y. Spiegel, J. Duchaine, and F. Torregrosa: Simulation of Plasma Immersion Ion Implantation

12th International Workshop on Junction Technology IWJT2012, Shanghai, China, May 14-15, 2012

- F. Cristiano, Z. Essa, Y. Qiu, Y. Spiegel, F. Torregrosa, J. Duchaine, P. Boulenc, C. Tavernier, O. Cojocaru, D. Blavette, D. Mangelinck, P. F. Fazzini, M. Quillec, M. Bazizi, M. Hackenberg, S. Boninelli: Implantation-induced structural defects in highly activated USJs: Boron precipitation and trapping in pre-amorphised silicon (**invited presentation**)

E-MRS Spring Meeting, Strasbourg, France, May 14-18, 2012:

- Z. Essa, C. Gaumer, A. Pakfar, M. Gros-Jean, M. Juhel, P. Boulenc, and C. Tavernier: Evaluation and modelling of lanthanum diffusion in TiN/La_2O_3/HfSiON/SiO_2/Si high-k stacks
- G. Fisicaro, K. Huet, R. Negru, J. Venturini, M. Hackenberg, P. Pichler, and A. La Magna: Boron pile-up in implanted silicon induced by submicrosecond laser annealing

19th International Conference on Ion Implantation Technology, Valladolid, Spain, June 25-29, 2012:

- A. Burenkov, A. Hahn, Y. Spiegel, H. Etienne, and F. Torregrosa: Simulation of BF_3 Plasma Immersion Ion Implantation into Silicon
- Z. Essa, F. Cristiano, Y. Spiegel, P. Boulenc, M. Quillec, N. Taleb, A. Burenkov, M. Hackenberg, E. Bedel-Pereira, V. Mortet, and C. Tavernier: BF3 PIII modelling: implantation, amorphisation and diffusion
- M. Hackenberg, P. Pichler, K. Huet, R. Negru, J. Venturini, G. Fisicaro, and A. La Magna: Modeling boron profiles after pulsed excimer laser annealing
- C. Nyamhere, F. Olivie, F. Cristiano, Z Essa, D. Bolze and Y. Yamamoto: Electrical characterization of {311} defects and related junction leakage currents in n-type Si after ion implantation
- F. Cristiano, Z. Essa, Y. Qiu, Y. Spiegel, F. Torregrosa, P. Boulenc, C. Tavernier, O. Cojocaru, D. Blavette, D. Mangelinck, and P. F. Fazzini: Residual structural defects in

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[20] http://www.atemox.eu/AtemoxTCADworkshopSlides.pdf

highly activated implanted USJs by advanced processes: millisecond annealing and plasma implants (**invited presentation**)

- G. Fisicaro, K. Huet, R. Negru, J. Venturini, M. Hackenberg, P. Pichler, and A. La Magna: Dynamics of dopant redistribution in molten silicon caused by laser irradiation

Conference on “Disorder in Order”, Cambridge, UK, September 19-20, 2012:

- S. Simdyankin and N.E.B. Cowern: High-entropy 'point' defects in diamond-structure materials

E-MRS Spring Meeting, Strasbourg, France, May 27-31, 2013:

- Z. Essa, F. Cristiano, O. Cojocaru-Mirédin, D. Mangelinck, D. Blavette, S. Duguay, N. Zographos, P. Boulenc and C. Tavernier: Continuum modelling of large boron-interstitial-clusters in silicon
- Z. Essa, F. Cristiano, Y. Spiegel, Y. Qiu, P. Boulenc, M. Quillec, N. Taleb, N. Zographos, E. Bedel-Pereira, V. Mortet, A. Burenkov, M. Hackenberg, F. Torregrosa and C. Tavernier: Large boron-interstitial clusters modelling in BF3 plasma implanted silicon (poster)
- G. Fisicaro, L. Pelaz, P. Lopez, M. Italia, K. Huet, F. Cristiano, Z. Essa, Q. Yang, E. Bedel-Pereira, and A. La Magna: Boron activation and defects dynamics in Si solid-phase during excimer laser annealing processes
- G. Fisicaro, K. Huet, R. Negru, M. Hackenberg, P. Pichler, M. Quillec, N. Taleb, and A. La Magna: Boron redistribution and activation in silicon liquid phase under excimer laser irradiation
- M. Hackenberg, P. Pichler, K. Huet, R. Negru, G. Fisicaro, A. La Magna, N. Taleb, M. Quillec: Simulation of the boron build-up formation during melting laser thermal annealing
- A. La Magna, G. Fisicaro, G. Nicotra, Y. Spiegel, F. Torregrosa: Atomic scale Monte Carlo simulations of BF3 Plasma Immersion Ion Implantation in Si
- C. Nyamhere, F. Cristiano, F. Olivie, E. Bedel-Pereira and Z. Essa: Electrical and optical characterization of extended defects induced in p-type Si after Si ion implantation
- Y. Qiu, F. Cristiano, Z. Essa, K. Huet, M. Quillec, G. Fisicaro and A. La Magna: Investigation of Large BICs formation in laser-annealed B+-implanted silicon (poster)
- A. Schenk and A. Scheinemann: Modeling of Leakage Currents in Ultra Shallow Junctions (invited)
- S. Simdyankin and N.E.B. Cowern: Extended point defects in silicon and other diamond-structure materials
- A. Tsibizov, A. Terterian, C. Zechner: Influence of Poisson equation boundary conditions, and quantum corrections to carrier concentrations at material interfaces in TCAD process simulation (poster)
- C. Zechner, N. Zographos, A. Tsibizov: Process Technology Simulation (invited)

16th International Workshop on Computational Electronics, Nara, Japan, June 4-7, 2013:

- A.Scheinemann and A. Schenk: Defect Analysis with TCAD-Based DLTS Simulation

18th Conference on Insulating Films on Semiconductors (INFOS 2013), Cracow, Poland, June 25-28, 2013:

- M. Hackenberg, P. Pichler, S. Baudot, Z. Essa, M. Gro-Jean, C. Tavernier, and S. Schamm-Chardon: Influence of La on the electrical properties of HfSiON: From diffusion to V_{fb} shifts (poster)

43rd European Solid-State Device Research Conference ESSDERC 2013, Bucharest, Romania, September 16-20, 2013:

- M. Hackenberg, M. Rommel, M. Rumler, J. Lorenz, P. Pichler, K. Huet, R. Negru, G. Fisicaro, A. La Magna, N. Taleb, M. Quillec: Melt Depth and Time Variations During Pulsed Laser Thermal Annealing with One and More Pulses

The International Conference on Simulation of Semiconductor Processes and Devices SISPAD 2013, Glasgow, UK, September 3-5, 2013:

- G. Fisicaro, L. Pelaz, M. Aboy, P. Lopez, M. Italia, K. Huet, F. Cristiano, Z. Essa,Q. Yang, E. Bedel-Pereira, M. Hackenberg, P. Pichler, M. Quillec, N. Taleb, and A. La Magna: Dopant dynamics and defects evolution in implanted silicon under laser irradiations: a coupled continuum and Kinetic Monte Carlo approach

15th International Conference on Gettering and Defect Engineering in Semiconductor Technology GADEST 2013, St John's College, Oxford, UK, September 23, 2013:

- N.E.B. Cowern, S.Simdyankin: Extended point-defects in Si and Ge

Publications in conference proceedings and periodicals:

- A. Burenkov, P. Pichler, J. Lorenz, Y. Spiegel, J. Duchaine, F. Torregrosa, Simulation of Plasma Immersion Ion Implantation, 2011 International Conference on Simulation of Semiconductor Processes and Devices - SISPAD 2011, Piscataway: IEEE, 231-234 (2011). DOI: 10.1109/SISPAD.2011.6034962
- F. Cristiano, Z. Essa, Y. Qiu, Y. Spiegel, F. Torregrosa, J. Duchaine, P. Boulenc, C. Tavernier, O. Cojocaru, D. Blavette, D. Mangelinck, P. F. Fazzini, M. Quillec, M. Bazizi, M. Hackenberg, S. Boninelli: Implantation-induced structural defects in highly activated USJs: Boron precipitation and trapping in pre-amorphised silicon, 2012 12th International Workshop on Junction Technology, edited by Yu-Long Jiang, Xin-Ping Qu, Guo-Ping Ru, and Bing-Zong Li, IEEE, 131-137 (2012). DOI: 10.1109/IWJT.2012.6212827
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- Z. Essa, C. Gaumer, A. Pakfar, M. Gros-Jean, M. Juhel, F. Panciera, P. Boulenc, C. Tavernier, F. Cristiano: Evaluation and modeling of lanthanum diffusion in TiN/La_2O_3/HfSiON/SiO_2/Si high-k stacks, Applied Physics Letters 101, 182901 (2012) DOI: 10.1063/1.4764558
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- N. E. B. Cowern, S. Simdyankin, C. Ahn, N. S. Bennett, J. P. Goss, J.-M. Hartmann, A. Pakfar, S. Hamm, J. Valentin, E. Napolitani, D. De Salvador, E. Bruno, S. Mirabella: Extended Point Defects in Crystalline Materials: Ge and Si, Physical Review Letters 110, 155501 (2013) DOI: 10.1103/PhysRevLett.110.155501
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Exploitation of results

The exploitation of the results achieved within ATEMOX is straight-forward. The main exploitation path goes via Synopsys who make the models developed commercially available to the nanoelectronics industry, research, and academia. ST will use them and the expertise gained by the dedicated research work to further drive their business on CMOS derivatives. Similarly, Excico and IBS will use the deeper understanding of physical effects gained by the dedicated research using their tools to promote the application of their equipment. The commercial availability of calibrated models to accompany the equipment is a further sales argument that directly stimulates a broader usage. For Probion and Semilab offering characterization support and tools, the experiences gained from research at the cutting edge of science and technology helped to improve their offerings and to attract new customers. Finally, the research partners Fraunhofer, CNR-IMM, CNRS, ETHZ, and Univ. Newcastle will use the knowledge gained in own research and research funded by third parties.

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